2. (Previously cancelled) The method set forth in claim 1 wherein forming an opening further comprises exposing a selected portion of the upper surface of the wafer to a reactive ion etching process for a preselected duration of time.

3. (Previously cancelled) The method set forth in claim 1 wherein depositing conductive material within the opening further comprises depositing at least one of copper, tungsten, nickel, and aluminum within the opening.

4. (Previously cancelled) The method set forth in claim 1 wherein depositing conductive material within the opening further comprises depositing a layer of conductive material over the upper surface of the wafer and within the opening, and removing a portion of the layer of conductive material overlying the upper surface of the wafer.

5. (Previously cancelled) The method set forth in claim 4 wherein removing a portion of the layer of conductive material further comprises performing a chemical mechanical polishing of the layer of conductive material to remove a portion of the layer of conductive material overlying the upper surface of the wafer.

6. (Previously cancelled) The method of claim 1 wherein forming a bump on an upper surface of the wafer further comprises forming a bump wherein at least a portion of a surface of the bump is wettable.

7. (Previously cancelled) The method of claim 1 wherein forming a contact pad on a lower surface of the wafer further comprises forming a contact pad wherein at least a portion of a surface of the contact pad is wettable.

8. (Previously cancelled) The method of claim 1 wherein forming an opening extending substantially through the wafer further comprises forming the opening extending substantially through a substrate of the wafer.

9. (Previously cancelled) The method of claim 8 wherein forming an opening extending substantially through the wafer further comprises forming the opening extending substantially through a substrate of the wafer and any additional process layers formed on the substrate.

10. (Previously cancelled) The method set forth in claim 1 wherein depositing conductive material within the opening further comprises depositing conductive material in contact with at least one conductive layer disposed within the wafer.

11. (Previously cancelled) A method for forming a stacked arrangement of a first and second wafer in an implantable device, comprising:

forming an opening extending substantially through the first wafer;

depositing conductive material within the opening to substantially fill the opening in the first wafer;

forming a bump on an upper surface of the first wafer adjacent the conductive material;

forming a contact pad on a lower surface of the first wafer adjacent the conductive material;

forming an opening extending substantially through the second wafer;

depositing conductive material within the opening to substantially fill the opening in the second wafer;

forming a bump on an upper surface of the second wafer adjacent the conductive material;

forming a contact pad on a lower surface of the second wafer adjacent the conductive material;

positioning the first wafer adjacent the second wafer with the bump of the first wafer being adjacent the contact pad of the second wafer; and

coupling the bump of the first wafer with the contact pad of the second wafer.

12. (Previously cancelled) The method set forth in claim 11 wherein coupling the bump of the first wafer with the contact pad of the second wafer further comprises soldering the bump of the first wafer with the contact pad of the second wafer.

13. (Previously cancelled) The method set forth in claim 11 wherein forming an opening in the first wafer further comprises exposing a selected portion of the upper surface of the first wafer to a reactive ion etching process for a preselected duration of time.

14. (Previously cancelled) The method set forth in claim 11 wherein depositing conductive material within the opening of the first wafer further comprises depositing at least one of copper, tungsten, nickel, and aluminum within the opening of the first wafer.

15. (Previously cancelled) The method set forth in claim 11 wherein depositing conductive material within the opening of the first wafer further comprises depositing a layer of conductive material over the upper surface of the first wafer and within the opening, and removing a portion of the layer of conductive material overlying the upper surface of the first wafer.

16. (Previously cancelled) The method set forth in claim 15 wherein removing a portion of the layer of conductive material further comprises performing a chemical mechanical polishing of the layer of conductive material to remove a portion of the layer of conductive material overlying the upper surface of the first wafer.

17. (Previously cancelled) The method of claim 11 wherein forming a bump on an upper surface of the first wafer further comprises forming a bump wherein at least a portion of a surface of the bump is wettable.

18. (Previously cancelled) The method of claim 11 wherein forming a contact pad on a lower surface of the second wafer further comprises forming a contact pad wherein at least a portion of a surface of the contact pad is wettable.

19. (Previously cancelled) The method of claim 11 wherein forming an opening extending substantially through the firs wafer further comprises forming the opening extending substantially through a substrate of the first wafer.

20. (Previously cancelled) The method of claim 19 wherein forming an opening extending substantially through the first wafer further comprises forming the opening extending substantially through the substrate of the first wafer and any additional process layers formed on the substrate.

21. (Previously cancelled) The method set forth in claim 11 wherein depositing conductive material within the opening of the first wafer further comprises depositing conductive material in contact with at least one conductive layer disposed within the first wafer.

22. (Currently amended) An implantable medical device, comprising:

a housing;

a semiconductor module mounted inside the housing and including first and second semiconductor die in a stacked arrangement, the stacked semiconductor die having circuitry implementing an operational implantable medical device function; and

a plurality of the electrical connections extending between the die, each electrical connection comprising an interconnection between a bump on an upper surface of the first die and a contact pad disposed on and extending away from a lower surface of the second die.

23. (Previously added) The device of claim 22 wherein the interconnection between a bump on an upper surface of the first die and a contact pad on a lower surface of the second die comprises a solder connection.

24. (Previously added) The device of claim 22 wherein the circuitry implements operational delivery of electrical stimulation therapy.

25. (Previously added) The device of claim 22 wherein the circuitry implements implantable pacemaker pacing and sensing functions.